Memory Trouble Relief Circuit

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor storage device for performing a redundancy relief in the semiconductor storage device.

2. Description of the related Art

With the progress of miniaturization of a semiconductor, the semiconductor including a semiconductor storage device has usually had a redundancy circuit to relieve the defect of a semiconductor device part. When a defect is detected in the storage device part upon inspection, the storage device part has been replaced by the redundancy circuit part to realize the improvement of a yield of the semiconductor. (JP-A-11-238393 or the like)

However, in the usual semiconductor including the semiconductor storage device, when the defect is not detected in the semiconductor storage device part upon inspection, a redundancy relief circuit is not used, so that leakage current is inconveniently generated even in the unused circuit.

SUMMARY OF THE INVENTION

The present invention is designed to solve the usual problem as described above, and aimed to provide a memory trouble relief circuit which can reduce the leakage current generated by unused redundancy circuit.

A first aspect of the memory trouble relief circuit of the invention is directed to a memory trouble relief circuit for relieving the failure of a memory of a semiconductor integrated circuit having the memory, comprising: a redundancy relief circuit having a redundancy circuit by which the defective part of the memory is replaced based on the diagnosed result of the memory; and a power line of different system from that of a power source for the semiconductor integrated circuit. According to this structure, the power sources of the semiconductor integrated circuit and redundancy relief circuit are provided in separate systems. Thereby, when the memory has no failure upon inspection of the semiconductor integrated circuit, it becomes possible not to supply power to the redundancy relief circuit. Thus, a leakage current generated in an unused redundancy circuit can be reduced.

A second aspect of the memory trouble relief circuit of the invention is directed to a memory trouble relief circuit for relieving the failure of a memory of a

semiconductor integrated circuit having the memory, said memory trouble relief circuit comprising: a self-diagnosis circuit for diagnosing the memory and outputting the diagnosed result to an external power control circuit and a redundancy relief circuit having a redundancy circuit by which the defective part of the memory is replaced based on the diagnosed result, wherein the supply of power to the redundancy relief circuit is controlled independently of the supply of power to the semiconductor integrated circuit by the power control circuit operating based on the diagnosed result. According to this structure, based on the self-diagnosis result, the supply of power to the redundancy relief circuit is controlled independently of the supply of power to the semiconductor integrated circuit. Therefore, when the memory has no failure upon inspection of the semiconductor integrated circuit, control is exercised so as not to supply power to the redundancy relief circuit. Thereby, the leakage current generated in the unused redundancy circuit can be reduced.

A third aspect of the memory trouble relief circuit of the invention is directed to a memory trouble relief circuit for relieving the failure of a memory of a semiconductor integrated circuit having the memory, comprising: a holding unit for previously holding a

diagnosed result of the memory upon inspection of the semiconductor integrated circuit and a redundancy relief circuit having a redundancy circuit by which the defective part of the memory is replaced based on the diagnosed result, wherein the supply of power to the redundancy relief circuit upon actual use of the semiconductor integrated circuit is controlled independently of the supply of power to the semiconductor integrated circuit by the power control circuit operating based on the diagnosed result. According to this structure, upon actual use of the semiconductor integrated circuit, the diagnosed result preheld upon inspection of the semiconductor integrated circuit is utilized to control the supply of power to the redundancy relief circuit independently of the supply of power to the semiconductor integrated circuit. Therefore, when the memory has no failure upon inspection of the semiconductor integrated circuit, control is exercised so as not to supply power to the redundancy relief circuit. Thereby, the leakage current generated in the unused redundancy circuit can be reduced.

In the second and third aspects of the memory trouble relief circuit of the invention, the power for the redundancy relief circuit is supplied from a different power source from that of the semiconductor integrated

circuit. According to this structure, the power source of the redundancy relief circuit is made different from the power source of the semiconductor integrated circuit, thereby reliably controlling the power for the redundancy relief circuit.

Besides, the self-diagnosis circuit outputs, to the power control circuit, the diagnosed result of the memory obtained as the self-diagnosis circuit operates every time power is turned on. According to this structure, the power is controlled based on the diagnosed result only when turned on, and can thereafter be used as usual.

In the invention, the defective part of the memory is replaced by means of fuse control. According to this structure, by utilizing the fuse control, the defective part of the memory can be reliably replaced by the redundancy circuit.

According to the invention, the power source for the redundancy relief circuit is independent of the power source for the semiconductor integrated circuit. Therefore, the supply of power to the redundancy relief circuit can be shut off when the memory has no failure. Thus, the leakage current generated in the unused redundancy circuit can be reduced.

BRIEF OF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram showing the structure of a memory trouble relief circuit according to a first embodiment of the present invention.

Fig. 2 is a diagram showing an operation flow of a memory trouble relief circuit according to a second embodiment of the present invention.

Fig. 3 is a diagram showing the structure of a memory trouble relief circuit according to a third embodiment of the present invention.

Fig. 4 is a diagram showing an operation flow of a memory trouble relief circuit according to a fourth embodiment.

DESCRIPTION OF THE PREFERED EMBODIMENTS

(First Embodiment)

Fig. 1 is a diagram showing the structure of a memory trouble relief device according to the first embodiment of the present invention.

The memory trouble relief device comprises a logic circuit 1 for realizing an actual function, a memory part 2 used by the logic circuit 1, a self-diagnosis circuit 3 for recognizing whether or not the failure of the memory part 2 is present, a redundancy circuit 4 for performing a replacement of the defective part of the memory part 2 by control of fuse or the like, on the basis of the

decided result of the self-diagnosis circuit 3, a comparator 5 for comparing the address of the memory designated by the logic circuit 1 with determination result (address which indicates the failure part) outputted from the redundancy circuit 3 and a selector 6 for selectively allowing the logic circuit 1 to access the redundancy relief circuit 4 when the memory is failed in accordance with the result of the comparator 5.

Power (1) is supplied to the logic circuit 1, the memory part 2, the self-diagnosis circuit 3 and the selector and power (2) is supplied to the redundancy circuit 4 and the comparator 5. A power control circuit 10 controls a supply of the power (1) and the power (2) based on the result of the self-diagnosis circuit 3. The power control circuit is provided outside or inside a semiconductor chip.

Fig. 2 is a diagram showing the operation flow of a memory trouble relief device according to a second embodiment of the present invention. In the operation flow of the memory trouble relief device, when a power is turned on, the self-diagnosis circuit 3 operates to perform the self-diagnosis of the memory(S10), and determines the result of the self-diagnosis(S11). When the result that the memory has no failure is outputted, the power control circuit 10 controls the power source

of the power (2) to be turned OFF (S12). When the result that the memory has the failure is outputted, the result of the self-diagnosis is stored in the redundancy circuit 4 (S13), and next the power control circuit 10 controls the power source of the power (2) to be turned ON(S14). Since the result of the self-diagnosis is held while the power is turned on, if the self-diagnosis circuit 3 is operated once upon turning on the power, the power (2) will not be controlled after that.

According to the first embodiment, the power sources of the semiconductor integrated circuit and redundancy relief circuit are provided in separate systems. Thereby, when the memory has no failure upon inspection of the semiconductor integrated circuit, it becomes possible not to supply power to the redundancy relief circuit. Thus, a leakage current generated in an unused redundancy circuit can be reduced.

(Second Embodiment)

Fig. 3 is a block diagram showing the structure of a memory trouble relief circuit according to the second embodiment of the invention. The description will be made with like reference numerals given to the same parts as in Fig. 1. In Fig. 3, the memory trouble relief circuit comprises a logic circuit 1, a memory part 2, a redundancy

circuit 4, a Flash memory 9 for holding the inspected result of a semiconductor integrated circuit, a comparator 5 for comparing an address designated by the logic circuit 1 with a decided result stored in the Flash memory 9, a selector 6 for enabling the logic circuit 1 to access the redundancy circuit 4 when the compared result of the comparator 5 indicates that the memory part 2 has a defective memory cell.

Power (1) is supplied to the semiconductor integrated circuit having the logic circuit 1, memory part 2 and selector 6. Power (2) is supplied to a redundancy relief circuit having the redundancy circuit 4 and comparator 5. A power control circuit 10 controls the supply of the powers (1) and (2) based on the result of evaluating the memory, held by the Flash memory 9.

Fig. 4 is a diagram showing the operation flow of a memory trouble relief device according to a fourth embodiment of the present invention.

The operation flow of the memory trouble relief device may be roughly divided into a semiconductor inspection step and an actual use. In the inspection step of the semiconductor, the test of the memory part 2 is performed (S20) and the inspected results about the presence or absence of the defect or failure of the memory and the defective part of the memory are stored in a Flash memory

9 in the semiconductor (S21). Upon actual use, the inspected result is determined by using the presence or absence of the defect or failure of the memory stored in the Flash memory 9(S22). When the defect or failure of the memory exists, the power control circuit 10 performs a control for turning the power (2) ON (S23). When the defect or failure of the memory does not exist, the power control circuit 10 performs a control for turning the power (3) OFF (S24).

According to the second embodiment, the power sources of the semiconductor integrated circuit and redundancy relief circuit are provided in separate systems. The presence or absence of the defect or failure of the memory part, which is the result obtained upon inspection, is stored in the Flash memory. Thus, upon actual use, control is exercised so as not to supply power to the redundancy circuit depending on the presence or absence of the defect or failure of the memory part. Thereby, an unused redundancy circuit can be prevented from generating a leakage current.

The first and second embodiments have described the case in which the supply of power to the redundancy relief circuit is controlled such that the power (2) is turned on if the memory has a failure and the power (2) is turned off if the memory has no failure. However, the

structure may be made as follows. If the memory has no failure, a power source line for supplying the power (2) is cut by trimming, so as not to supply the power to the redundancy relief circuit.

The memory trouble relief circuit of a semiconductor integrated circuit according to the present invention can control the power depending on the presence or the absence of the failure of the memory. When the failure of the memory does not exist, unnecessary leakage current can be reduced in an unused redundancy relief circuit part and consumed current can be effectively reduced in the semiconductor integrated circuit on which the memory is mounted. Especially, the memory trouble relief circuit is useful for portable terminal equipment requested for low consumed current.